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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,111	12/29/2000	Wendell P. Noble JR.	M4065.0019/P019-A	6297

24998 7590 05/11/2004

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EXAMINER	
ROSE, KIESHA L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,111	NOBLE ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,23-33 and 55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE filed 19 February 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble et al. (U.S. Patent 5,973,356).

Noble discloses a memory device (Figs. 3,12,13 and 20) that comprises a SRAM that contains two complementary gated vertically stacked bipolar transistors (300) where the transistors comprise p-n-p and n-p-n transistors (310/320/315) sharing their

central n and p regions and configured to exhibit two bistable current states for storing information, one of the current states being achieved by operation of gate-induced latchup of transistors that results in the memory cell having lowered resistance, the two transistors including a first gate (335/YG1) and a second gate (325,XG2) operational to induce latchup and the first and second gates being connected to a respective first vertical side and a second vertical side of vertically stacked bipolar transistors, the first gate spans the central n- region of the p-n-p transistor and the second gate spans the central p- region of the n-p-n transistor and are orthogonally positioned relative to each other, where the transistor is formed on a supporting substrate (305) in a trench.

Claims 17-20, 23-27 and 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble et al. (U.S. Patent 5,973,356).

Noble discloses a memory device (Figs. 3,12,13 and 20) that comprises a SRAM that contains vertically stacked transistors (300) that having a first p-region (305), a first n-region (310), a second p-region (320) and second n-region (315), a first gate (335) bridging first and second p-regions across the first n-region (connecting central n-regions) and a second gate (325) bridging first and second n-region across the second p-region (connecting central p-regions), a row address line (YG1) (fourth gate line not located in trench and connecting lower p-regions of transistors) in electrical communication with first p-region, a column address line (XD2) (third gate line not located in trench connecting upper n-regions of the transistors) in electrical communication with second n-region, a write row address line (335) forming a first gate for gating charge between first and second p-regions, a column write address line

(XG2/325) forming second gate for gating charge between first and second n-regions, where the first and second gates are configured to produce latchup when a voltage pulse is provided to both of the gates in vertical transistor stack as a current state for storing information in SRAM, the gates are orthogonally positioned relative to each other, where the transistor is formed on a supporting substrate SOI (305) made of a substrate, insulating layer (oxide) and semiconductor layer where the transistors are formed in trenches.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble.

Noble discloses the memory cells having an area of F^2 (Abstract), but the Noble reference does not disclose the area to be 4 F^2. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the area of the memory cell to be 4 F^2, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (1980).

Claims 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble and further in view of Shirley (US Publication 2004/0062110).

Noble discloses a memory device (Figs. 3,12,13 and 20) that comprises a memory circuit that contains a SRAM memory cell that has at least two gated complementary vertically stacked bipolar transistors (300) where the transistors comprise p-n-p and n-p-n transistors (310/320/315) sharing their central n and p regions and configured to exhibit two bistable current states for storing information, one of the current states being achieved by operation of gate-induced latchup of transistors where the collector region of the p-n-p is connected to the base region of the n-p-n, a first gate (335/YG1) and a second gate (325,XG2) operational to induce latchup when gates are turned on and the first gate spans the n- region of the p-n-p transistor and the second gate spans the p-region of the n-p-n transistor and are orthogonally positioned relative to each other. In regards to claim 33, the memory cells have an area of F^2 (Abstract), but the Noble reference does not disclose the area to be 4 F^2. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the area of the memory cell to be 4 F^2, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (1980). Noble discloses all the limitations except for a computer system with a processor connected to the memory circuit. Whereas Shirley discloses a SRAM (Fig. 5) that contains a computer system with a processor (104) connected to the memory circuit (408). The computer system is added to process the stored information of the memory cells. (Page 4, Paragraph 30/31)

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a computer system to process the stored information of the memory cells as taught by Shirley.

Response to Arguments

Applicant's arguments with respect to claims 1-20, 23-33 and 55 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

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